



# AKASH INSTITUTE OF ENGINEERING AND TECHNOLOGY

Affiliated to Visvesvaraya Technological University, Belagavi and Approved by AICTE, New Delhi.

Devanahalli, Bengaluru- 562110 [www.akashiet.com](http://www.akashiet.com)



***Mandatory Disclosure***

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Devanahalli, Bangalore Rural- 562110 [www.akashiet.com](http://www.akashiet.com)

### **Vision**

"To be globally acclaimed Institute in technical education, management and research for holistic socio-economic development".

### **Mission**

- M1. Impart fundamental knowledge in engineering, applied science and develop advanced skills to achieve professional excellence.
- M2. Promote research culture among students and faculty.
- M3. Inculcate ethical, spiritual values and sense of social responsibility for overall personality development.

## Mandatory Disclosure

### 1. Name of the Institution

#### **Akash Institute of Engineering and Technology**

Prasannahalli Main Road, Devanahalli

Bengaluru Rural– 562110, Karnataka

Mobile No. : +91-9743873555

Email : [akshtechnical23@gmail.com](mailto:akshtechnical23@gmail.com) principal@akashiet.com

### 2. Name and address of the Trust/Society/Company and the Trustees

#### **Akash Education and Development Trust**

Ward No. 22, Prashanth Nagar, Devanahalli

Bengaluru Rural– 562110, Karnataka

### 3. Name and Address of the Principal

#### **Dr. Prakash S Dabeer**

Akash Institute of Engineering and Technology,

Prasannahalli Main Road, Devanahalli

Bengaluru Rural– 562110, Karnataka

Mobile No.: +91-9743873555

Email: principal@akashiet.com

### 4. Name of the Affiliating University

#### **VISVESVARAYA TECHNOLOGICAL UNIVERSITY**

Jnanasangama Campus, Machhe,

Belagavi -590 018, Karnataka.

## 5. Governance

### 5.1 Governing Council

#### List of Governing Council Members

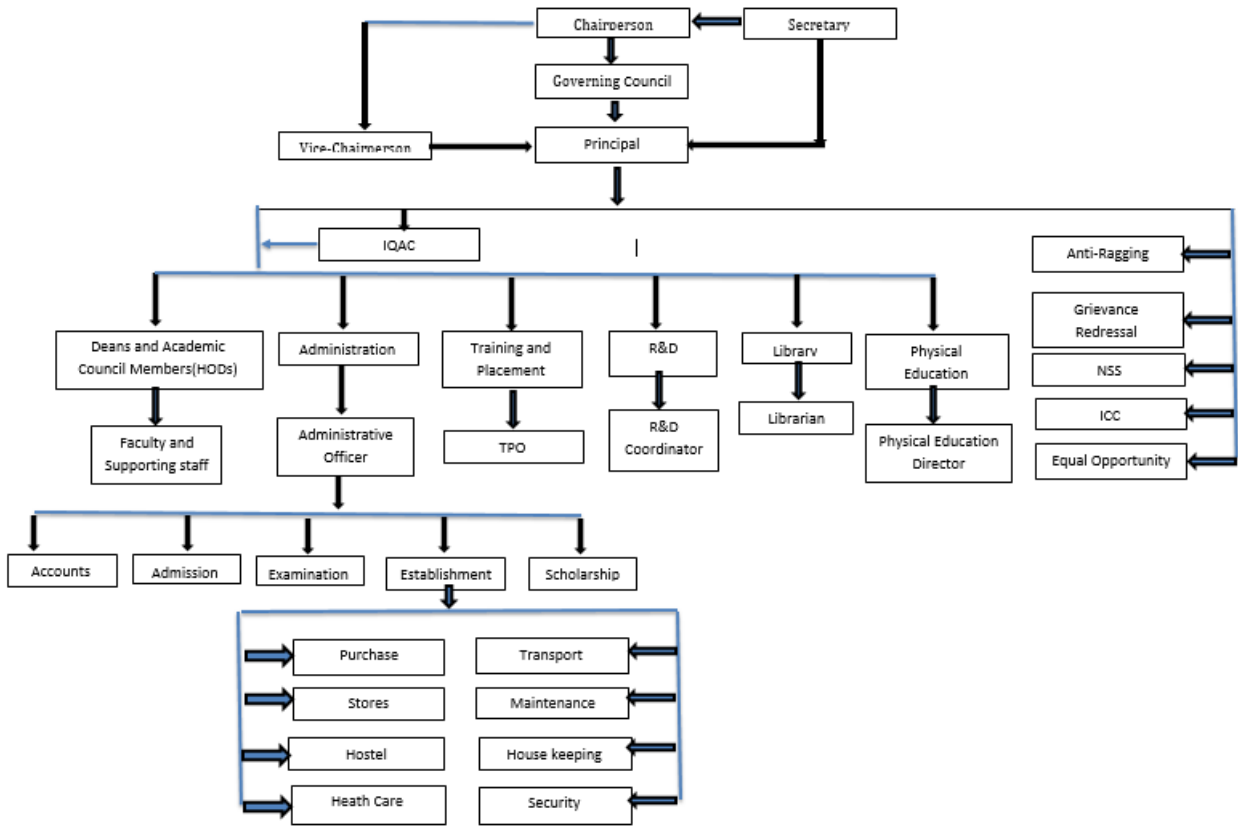
Sl. No.	Members as per AICTE	Name of the member
1	Chairperson	Smt. Pushpa Muniraju Chairperson, Akash Group of Institution Devanahalli, Bengaluru-562110
2	Secretary	Sri. K. Muniraju Secretary, Akash Group of Institution Devanahalli, Bengaluru-562110
3	Vice-Chairman	Sri. Amar Gowda Vice-Chairman, Akash Group of Institution Devanahalli, Bengaluru-562110
4	Member	Sri. Prabhakar H Ramdas Chief Finance Officer, Akash Group of Institution Devanahalli, Bengaluru-562110
5	Nominee of the Visvesvaraya Technological University, Belagavi	Nominee, Visvesvaraya Technological University, Belagavi
6	Nominee of the All India Council for Technical Education (AICTE)	R.O. / Nominee, AICTE-SWRO, Bengaluru
7	Nominee of the State Government	Director Directorate of Technical Education
8	Industrialist	Mr. Vijay Kumar S Makal Proprietor Essem Powder Coatings, Bengaluru and President, Bangalore Powder Coated Association
9	Member Secretary	Dr. Prakash S Dabeer Principal, Akash Institute of Engineering and Technology Devanahalli, Bengaluru-562110
10	Faculty member	Dr. Pranesh K G Associate Professor, Dept. of Mechanical Engineering Akash Institute of Engineering and Technology Devanahalli, Bengaluru-562110
11	Faculty member	Dr. Santhosh T C M Associate Professor, Dept. of Physics Akash Institute of Engineering and Technology Devanahalli, Bengaluru-562110

## 5.2 Member of Academic Advisory Body


Akash Institute of Engineering and Technology is having an academic council with the following members.

Sl No.	Name of the Members	Designation	Qualification
1	Dr. Prakash S Dabeer Principal, Akash Institute of Engineering and Technology	Chairman	Ph.D.
2	Dr. Pranesh K G HOD- Mechanical Engineering	Member	Ph.D.
3	Dr. Sridhar C S HOD_CSE(AIML)	Member	Ph.D.
4	Dr. Somanath J Patil HOD-Computer Science and Engineering	Member	Ph.D.
5	Mrs. Roopa G HOD-Information Science and Engineering	Member	M.Tech (Ph.D.)
6	Mr. Anil Kumar Warad HOD-Artificial Intelligence and Data Science	Member	M.Tech (Ph.D.)
7	Mr. Praveen P HOD-Computer Science and Engineering (Data Science)	Member	M.Tech (Ph.D.)
8	Mrs. Nagamma HOD-Computer Science and Engineering (Cyber Security)	Member	M.Tech (Ph.D.)
9	Mr. Sunil Kumar B S HOD-Electronics and Communication Engineering	Member	M.Tech (Ph.D.)
10	Dr. Santhosh T C M HOD- Physics	Member	Ph.D.

### 5.3 Organizational Chart and Processes



## 5.4 Establishment of Anti Ragging Committee –Yes



**AKASH INSTITUTE OF ENGINEERING AND TECHNOLOGY**  
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 Devanahalli, Bengaluru- 562110, www.akashiet.com

Ref. No. \_\_\_\_\_ Date:04-10-2025

**Office Order**

This institute has nominated the following members for the anti-ragging committee. This order will come into effect from 04.10.2025 until further orders.

Sl No.	Name	Designation & Department	Role
1.	Dr. Prakash S Dabeer	Principal	Chairman
2.		Police Inspector, Devanahalli Town	Special Invitee
3.	Mr. Sunil Kumar B S	Assistant Professor (ECE)	Convenor
4.	Mr. Chetan	General Administrator	Member
5.	Mr. Ibrahim	Director Physical Education & Sports.	Member
6.	Dr. Sridhar C S	HOD, Department of AIML	Member
7.	Dr. Somnath Patil	HOD, Department of CSE	Member
8.	Dr. Sri hari	HOD, Department of MBA	Member
9.	Mr. Anil K Warad	HOD, Department of AI & DS	Member
10.	Mrs. Roopa G	HOD, Department of ISE	Member
11.	Mrs. Nagamma C Y	HOD, Department of CY	Member
12.	Mr. Vijay Kumar Y M	HOD, Department of DS	Member
13.	Mr. Madhu N	HOD, Department of MCA	Member
14.	Mr. Prajwal Gowda	Chief Warden	Member
15.	Student Representatives: Mr. Arvind P (AIML 3 <sup>rd</sup> year) Ms. Shravanthi L (AI & DS 3 <sup>rd</sup> Year)	Boy Student Girl Student	Student Members

**Functions:**


- Monitoring ragging preventions in and around the campus.
- Monitoring anti-drugs activities around the college campus.
- Ensure that the guidance from the regulatory bodies is followed to curb the menace of ragging in the institute campus and Hostels.

**Terms:**


- Two years an shall continue until further reconstitution

**Meeting Frequency:**

Every Semester and may be schedules as and when required.

  
**PRINCIPAL**  
 AKASH INSTITUTE OF ENGINEERING AND TECHNOLOGY  
 Prasannahalli Main Road,  
 Devanahalli, Bangalore-562110.

**5.5 Establishment of Online Grievance Redressal Mechanism – Yes**



**AKASH INSTITUTE OF ENGINEERING AND TECHNOLOGY**  
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 Prasanna Halli Main Road, Devanahalli, Bengaluru-562110

02/09/2024

**OFFICE ORDER**

**STUDENT GRIEVANCE REDRESSAL COMMITTEE**

The Students Grievance Redressal Committee(SGRC) Constituted in the College to address and resolve any issue/grievance raised by the students within the preview of the institution norms.

Sl. No.	Name	Designation and Department	Role	Contact Number	Email ID
01	Dr. Prakash S Dabeer	Principal	Chairman	9860676940	Principal@akashiet.com
02		VTU Nominee	Member		
03	Dr. Santhosh T C M	Assistant Professor	Member/ Convenor	7899250264	Santhosh@akashiet.com
04	Prof. Shravani M A	Assistant Professor	Member	8904136676	shravanianjaneyareddy@gmail.com
05	Dr. Shiva Reddy G V	Assistant Professor	Member	8310403107	Shivareddy.g.v@gmail.com
06	Prof. Sneha C	Assistant Professor	Member	8549932772	Snehacsneha97@gmail.com
07	Mr. Chetan N	Administrator	Member	8310434645	

**Copy to:**

1. All the faculty members of AIET
2. All HODs
3. HR Department
4. Office file

*(Signature)*  
Principal  
**PRINCIPAL**  
**AKASH INSTITUTE OF ENGINEERING & TECHNOLOGY**  
 Prasannahalli Main Road, Devanahalli  
 Bengaluru - 562 110.

**5.6 Establishment of Grievance Redressal Committee in the Institution and Appointment of OMBUDSMAN by the University – Yes (VTU SHALL appoint OMBUDSMAN)**

## 5.7 Establishment of Internal Complaint Committee(ICC) – Yes



# AKASH INSTITUTE OF ENGINEERING & TECHNOLOGY

(Unit of Akash Education & Development Trust)  
Prasannahalli Main Road, Near International Airport, Devanahalli, Bengaluru - 562 110  
Ph : +91 9743873555 | Email : akashtechical23@gmail.com | Web : www.akashiet.com

Ref. No. AFDT/AIET/ANTI SEXUAL HARR/2025-26/ 308

Date: 01 AUG 2025

### OFFICE ORDER

#### CONSTITUTION OF COLLEGE INTERNAL COMPLAINT COMMITTEE

The College Internal Complaint Committee constituted in the college to address and resolve any issue/Complaints raised by students, faculty and staff within the preview of the institution norms. The Members of the Committee are as follows:

Sl. No.	Name	Designation & Department	Role
1	Mrs. Pushpa M	Chairperson, AGI	Chairperson
2	Dr. Prakash S Dabeer	Principal	Chairman
3	Mrs. Varsha T R	Assistant Professor, MBA	Co-ordinator
4	Mrs. Latha	Administrative officer.	Member
5	Mrs Nagamma	Assistant Professor, Dept. of CSE(CY)	Member
6	Mrs. Roopa G	Assistant Professor, Dept. of ISE	Member
7	Ms. Chithrashree J N	Assistant Professor, Dept. of Basic Sciences.	Member
8	Ms. Bhavya C M	Student, CSE	Student Member
9	Ms. Poorvika	Student, AI&DS	Student Member

#### **FUNCTIONS:**

- Prevent discrimination and sexual harassment by promoting gender amity among students and employees.
- Deal with cases of discrimination and sexual harassment against women, in a time bound manner, aiming at ensuring support services to the victimised and termination of harassment.
- To treat sexual harassment as a misconduct and initiate punitive actions for such misconduct.
- To provide conducive environment and congenial atmosphere in the campus.
- To assist the aggrieved woman to place the complaint.
- Maintain Confidentiality in all aspects of any proceedings of the committee.
- Recommended appropriate redressal and punitive action against the guilty to the management.

Copy to:

1. All Faculty Members of AIET
2. All HODs
3. HR Department
4. Office File

  
 Dr. Prakash S Dabeer  
**PRINCIPAL**  
 AKASH INSTITUTE OF ENGINEERING AND TECHNOLOGY  
 Prasannahalli Main Road,  
 Devanahalli, Bangalore-562110.


**5.8 Internal Quality Assurance Cell – Yes****AKASH INSTITUTE OF ENGINEERING AND TECHNOLOGY**

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26/12/2025

**Internal Quality Assurance Cell (IQAC)****IQAC Core Committee**

Sl. No	Name of the Faculty	Designation	Role
1	Dr. Prakash S Dabeer	Principal	Chairperson
2	Mr. Amar Gowda	Vice Chairman Akash Group of Institution	Management Representative -Member
3	Dr. Pranesh K G	Associate Professor and HOD-Mechanical Engineering	Coordinator
4	Dr. Santhosh TC M	Associate Professor and First Year Coordinator.	Member
5	Mr. Anil Kumar Warad	Assistant Professor and HOD-Artificial Intelligence and Data Science	Member
6	Mr. Mahesh Mokshith M L	Assistant Professor Dept. of Mechanical Engineering	Member
7	Ms. Bhavya C M 5 <sup>th</sup> Semester-CSE	Student Representative	Member

  
Dr. Prakash S Dabeer

**PRINCIPAL**

AKASH INSTITUTE OF ENGINEERING AND TECHNOLOGY  
Prasannahalli Main Road,  
Devanahalli, Bangalore-562110.

Copy to

1. Administrative officer, AIET
2. All HODs, AIET
3. All Faculty members, AIET

## 6. Programmes

### 6.1 Name of Programmes approved by AICTE 2025-26

Sl No.	Level	Name of the Programme	Course	Intake
1	Under Graduate	Engineering and Technology	Artificial Intelligence (AI) and Data Science	180
2	Under Graduate	Engineering and Technology	Computer Science & Engineering	180
3	Under Graduate	Engineering and Technology	Computer Science and Engineering (Artificial Intelligence and Machine Learning)	180
4	Under Graduate	Engineering and Technology	Computer Science and Engineering (Cyber Security)	120
5	Under Graduate	Engineering and Technology	Computer Science and Engineering (Data Science)	30
6	Under Graduate	Engineering and Technology	Electronics and Communication Engineering	90
7	Under Graduate	Engineering and Technology	Information Science and Engineering	90
8	Under Graduate	Engineering and Technology	Mechanical Engineering	30
9	Post Graduate	Management	MBA	60
10	Post Graduate	Computer Applications	MCA	60

### 6.2 Total number of Courses

Under Graduate :08

Post Graduate :02

**6.3 Programme: Name/ number of seat/duration**

SI No.	Name of the Programme	Number of Seats	Duration
1	Artificial Intelligence (AI) and Data Science	180	4
2	Computer Science & Engineering	180	4
3	Computer Science and Engineering (Artificial Intelligence and Machine Learning)	180	4
4	Computer Science and Engineering (Cyber Security)	120	4
5	Computer Science and Engineering (Data Science)	30	4
6	Electronics and Communication Engineering	90	4
7	Information Science and Engineering	90	4
8	Mechanical Engineering	30	4
9	MBA	60	2
10	MCA	60	2

**6.5 Fee (as approved by the state government)**

Under Graduation: Tuition fee Rs.1,12,410/-

Post Graduate: Tuition fee Rs. 69,310 /-

## 7. Faculty

### 7.1 Course/Branch wise list Faculty Members List

Sl.No	Name of the faculty	Designation	Department
1	Dr. Pranesh K G	Associate Professor	Mechanical Engineering
2	Dr. Shashikanth G S	Associate Professor	Mechanical Engineering
3	Mr. Mahesh Mokshith M L	Assistant Professor	Mechanical Engineering
4	Mr.Bhuvan Athresh	Assistant Professor	Mechanical Engineering
5	Mr.Babu K N	Assistant Professor	Mechanical Engineering
6	Dr. Somanath J Patil	Associate Professor	Computer Science & Engineering
7	Ms. Suhasini	Assistant Professor	Computer Science & Engineering
8	Ms. Ankitha Y M	Assistant Professor	Computer Science & Engineering
9	Mrs. Shyla	Teaching Assistant	Computer Science & Engineering
10	Mrs. Roopa G	Assistant Professor	Information Science and Engineering
11	Mrs. Preethi S P	Teaching Assistant	Information Science and Engineering
12	Dr.Sridhar C S	Professor	Computer Science and Engineering (AIML)
13	Mr.Venkatesh K	Assistant Professor	Computer Science and Engineering (AIML)
14	Ms. Harshitah G J	Teaching Assistant	Computer Science and Engineering (AIML)
15	Ms. Kavya	Teaching Assistant	Computer Science and Engineering (AIML)
16	Mr. Anil Kumar Warad	Assistant Professor	Artificial Intelligence (AI) and Data Science
17	Mr. Manohar	Assistant Professor	Artificial Intelligence (AI) and Data Science

18	Ms. Harsha S	Assistant Professor	Artificial Intelligence (AI) and Data Science
19	Ms. Lavanya K V	Teaching Assistant	Artificial Intelligence (AI) and Data Science
20	Mrs. Nagamma	Assistant Professor	Computer Science and Engineering (Cyber Security)
21	Mr. Sunil Pandit	Assistant Professor	Computer Science and Engineering (Cyber Security)
22	Mr. Prveen P	Assistant Professor	Computer Science and Engineering (Data Science)
23	Mrs.Sumitha Raj	Assistant Professor	Computer Science and Engineering (Data Science)
24	Mr. B S Sunil Kumar	Assistant Professor	Electronics and Communication Engineering
25	Mr. Shiva Kumar	Assistant Professor	Electronics and Communication Engineering
26	Ms. Yashaswini	Assistant Professor	Electronics and Communication Engineering
27	Mr. Chandrakanth	Assistant Professor	Electronics and Communication Engineering
28	Dr. Santhosh T C M	Associate Professor	Physics
29	Mrs. Chaitrashree J N	Assistant Professor	Physics
30	Mrs.Vasantha	Assistant Professor	Physics
31	Ms. Deepa	Assistant Professor	Physics
32	Dr. Praveen Kumar M	Assistant Professor	Mathematics
33	Dr.Megha M Manakame	Assistant Professor	Mathematics
34	Mr. Pramod Gowda	Assistant Professor	Mathematics
35	Mrs. Mamatha S	Assistant Professor	Mathematics

36	Mr. Sudhakar	Assistant Professor	Mathematics
37	Mrs. Premalatha	Assistant Professor	Mathematics
38	Ms.Sneha H	Assistant Professor	Mathematics
39	Dr. Shiva Reddy	Assistant Professor	Chemistry
40	Mr. Hemantha T	Assistant Professor	Chemistry
41	Ms. Krupa	Assistant Professor	Chemistry
42	Ms. Kusuma	Assistant Professor	Chemistry
43	Dr. Sri Hari	Associate Professor	MBA
44	Mrs. Varsha T R	Assistant Professor	MBA
45	Ms. Archana	Assistant Professor	MBA
46	Mr.Maltesh Kulakarni	Assistant Professor	MBA
47	Dr.Mithun	Assistant Professor	MBA
48	Mr. Madhu N	Assistant Professor	MCA
49	Ms. Meghana	Assistant Professor	MCA
50	Ms.Pratiksha Natikkar	Assistant Professor	MCA
51	Mr.Venugopal	Assistant Professor	MCA
52	Ms. Aishwarya patil	Assistant Professor	MCA
53	Ms. Jayashree	Assistant Professor	MCA
54	Mrs. Charishma	Assistant Professor	English
55	Mr.Anjappa B V	Assistant Professor	Kannada
56	Mrs. Sindhu G A	Assistant Professor	Humanities
57	Mrs. Aakruti Singh	Assistant Professor	Humanities
58	Mr. Ibrahim M	Physical Education Director	Physical Education
59	Mr. Shankara M N	Librarian	Library

**7.2 Permanent Faculty – 59**

**7.3 Permanent Faculty: Student Ratio: 1:19**

## **8. Profile of Principal**

**Name:** Dr. Prakash S Dabeer

**Date of Birth:** 18-08-1966

**Education Qualifications:** BE, ME, Ph.D.

### **Work Experience**

**Teaching:** 35years

**Research:** 10 years

**Administration:** 22 Years (As a Principal: 12 years and as a HOD: 10 years)

**Industry :** 01 year

**Area of Specialization:** Optimisation Techniques and Design of Experiments

**Courses taught at Under Graduate/ Post Graduate Level:** Mechanical Engineering subjects

**Research guidance (Number of Students):** 02

**No. of papers published in National/International Journals/Conferences:** 65

**Projects Carried out:** AICTE-MODROB (Modernization of Computer Integrated Manufacturing (CIM) Lab)

## 9. Admission

### 9.1 Number of seats sanctioned with the year of approval

Sl.No	Department	Sanctioned intake	Year of Establishment	Approved up to
1	Artificial Intelligence (AI) and Data Science	180	2023-24	2025-26
2	Computer Science & Engineering	180	2023-24	2025-26
3	Computer Science and Engineering (Artificial Intelligence and Machine Learning)	180	2023-24	2025-26
4	Computer Science and Engineering (Cyber Security)	120	2023-24	2025-26
5	Computer Science and Engineering (Data Science)	30	2023-24	2025-26
6	Electronics and Communication Engineering	90	2023-24	2025-26
7	Information Science and Engineering	90	2023-24	2025-26
8	Mechanical Engineering	30	2023-24	2025-26
9	MBA	60	2023-24	2025-26
10	MCA	60	2023-24	2025-26

**9.2 Admission UG and PG :AY 2025-26**

<b>Sl. No.</b>	<b>Level</b>	<b>Name of the Programme</b>	<b>Course</b>	<b>Intake</b>	<b>Admitted</b>
1	Under Graduate	Engineering and Technology	Artificial Intelligence (AI) and Data Science	180	124
2	Under Graduate	Engineering and Technology	Computer Science & Engineering	180	136
3	Under Graduate	Engineering and Technology	Computer Science and Engineering (AIML	180	168
4	Under Graduate	Engineering and Technology	Computer Science and Engineering (Cyber Security)	120	45
5	Under Graduate	Engineering and Technology	Computer Science and Engineering (Data Science)	30	23
6	Under Graduate	Engineering and Technology	Electronics and Communication Engineering	90	39
7	Under Graduate	Engineering and Technology	Information Science and Engineering	90	50
8	Under Graduate	Engineering and Technology	Mechanical Engineering	30	02
9	Post Graduate	Management	MBA	60	46
10	Post Graduate	Computer Applications	MCA	60	41

**9.3 Number of applications received during last year for admission under Management Quota and number admitted AY:2025-26**

Sl. No.	Level	Name of the Programme	Course	Application Received	Admitted
1	Under Graduate	Engineering and Technology	Artificial Intelligence (AI) and Data Science	52	47
2	Under Graduate	Engineering and Technology	Computer Science & Engineering	63	56
3	Under Graduate	Engineering and Technology	Computer Science and Engineering (AIML)	126	99
4	Under Graduate	Engineering and Technology	Computer Science and Engineering (Cyber Security)	22	11
5	Under Graduate	Engineering and Technology	Computer Science and Engineering (Data Science)	15	12
6	Under Graduate	Engineering and Technology	Electronics and Communication Engineering	29	21
7	Under Graduate	Engineering and Technology	Information Science and Engineering	33	29
8	Under Graduate	Engineering and Technology	Mechanical Engineering	11	01
9	Post Graduate	Management	MBA	38	33
10	Post Graduate	Computer Applications	MCA	32	29

## **10. Admission Procedure**

### **10.1 Mention the admission test being followed, name and address of the Test Agency/State Admission Authorities and its URL (website)**

CET - Karnataka Examination Authority, Sampige Road, Malleshwaram, Bangalore- 560012

<https://cetonline.karnataka.gov.in/kea/>

COMED K - # 132, Second Floor, 11th main, 17th cross, Malleshwaram, Bangalore 560055

<https://www.comedk.org/>

PGCET - KEA, Sampige Road, Malleshwaram, Bangalore- 560012

<https://cetonline.karnataka.gov.in/kea/>

**10.2 Number of seats allotted to different Test Qualified candidate separately (AIEEE//JEE/ CET (State conducted test/ University tests/ CMAT)/ Association conducted test etc.)  
AY:2025-26**

Sl. No.	Level	Name of the Programme	Course	CET	COMED K
1	Under Graduate	Engineering and Technology	Artificial Intelligence (AI) and Data Science	76	01
2	Under Graduate	Engineering and Technology	Computer Science & Engineering	79	01
3	Under Graduate	Engineering and Technology	Computer Science and Engineering (AIML)	67	02
4	Under Graduate	Engineering and Technology	Computer Science and Engineering (Cyber Security)	33	01
5	Under Graduate	Engineering and Technology	Computer Science and Engineering (Data Science)	11	00
6	Under Graduate	Engineering and Technology	Electronics and Communication Engineering	18	00
7	Under Graduate	Engineering and Technology	Information Science and Engineering	22	01
8	Under Graduate	Engineering and Technology	Mechanical Engineering	01	00
9	Post Graduate	Management	MBA	13	NA
10	Post Graduate	Computer Applications	MCA	12	NA

**10.3 Calendar for admission against Management/vacant seats:**

- The Institute follow the calendar in line with KEA and COMED K
- Open date of request for applications - 22.05.2025
- Last date for closing of admission –As per Admission authority of the State.
- Starting of the Academic session - As per VTU calendar of Events
- The waiting list shall be activated only on the expiry of date of main list - yes
- The policy of refund the Fee, in case of withdrawal, shall be clearly notified - yes

**11. Criteria and Weightages for Admission**

Passed second PUC/12th standard /equivalent examination with English as one of the languages and obtained a minimum of 45% of marks in aggregate in physics and mathematics along with chemistry/Biology/Bio-Technology / Electronics/Computer

**12. List of Applicants**

**12.1 List of candidate whose applications have been received along with percentile/percentages core for each of the qualifying examination in separate categories for open seats:** Maintained

**12.2 List of candidate who have applied along with percentage and percentile score for Management quota seats (merit wise):** Maintained

**13. Information of Infrastructure and Other Resources Available****13.1 Number of Class Rooms and size of each:**

Number of class rooms: 45    Size of each class room: 82.3 Sq.m

**13.2 Number of Tutorial rooms and size of each**

Number of Tutorial rooms:12    Size of each Tutorial room: 33 Sq.m

**13.3 Number of Laboratories and size of each**

Number of Laboratories:26    Size of each Laboratory: 66 Sq.m

**13.4 Number of Computer Centres with capacity of each:**

Number of computer centres: 01    Each lab capacity: 120

**13.5 Central Examination Facility, Number of rooms and capacity of each:**

Central Examination Facility: Available

Number of Rooms:45 Capacity of each room:34

**13.6 Barrier Free Built Environment for disabled and elderly persons: Yes**

**13.7 Hostel Facilities: Yes**

**13.8 Number of Library books/e-books/Titles/Journals available**

- Total Titles: 592
- Total Volumes: 4335
- E-books: 26790
- Journals:
- Magazines:

**13.9 List of online National/International Journals subscribed: VTU consortium**

**13.10 National Digital Library (NDL) subscription: Yes**

**13.11 List of Major Equipment/Facilities in each Laboratory/Workshop****For I & II year B.E.**

<b>Sl. No.</b>	<b>Name of the Laboratory/Workshop</b>	<b>Major Equipment Available</b>
1	Engineering Physics Lab	Function Generator, Four Probe Kit, Semiconductor Laser , Digital Travelling Microscope, Magnetic stirrer.
2	Engineering Chemistry Lab	Conductivity meter, Potentiometer, Colorimeter, Flame Photometer, pH Meter
3	EME Lab	Lathe machine, Milling Machine, Bench Grinder, Power Hacksaw, Welding, Bench Vice, Hand Tools, Surface plate, Hardness tester, Viscometer, Sinebar, Snip gauges
4	CAED Lab	60 Computers with Solid edge V20 Software Printers
5	Computer labs	570 Computers with Printing facility along with softwares such as Turbo c ++, Anaconda, Python, Code blocks, Solid Edge, Microsoft Office, Google Chrome, Oracle, Xilinx, Adobe reader, Java Exclipse, Lab view, Oracle Virtualbox (Fedora)
6	Analog and Digital System Design Lab	CROs, Function Generators, Regulated power supplies, Digital IC trainer kit, Transformers, Multimeters
7	Communication Lab	CROs, Function Generators, Dual Power supplies, DSOs, Multimeters
8	EC software lab	30 computers with softwares such as Matlab, LABVIEW/XILINX/Pspice
9	Language lab	20 Computers

**13.12 List of Experimental Setup in each Laboratory/Workshop**

<b>Sl. No.</b>	<b>Name of the Laboratory/Workshop</b>	<b>List of Experimental Setup</b>
1	Engineering Physics Lab	<ul style="list-style-type: none"> <li>• Series LCR Resonance Circuits</li> <li>• Charging and Discharging of Capacitor</li> <li>• Planck's Constant</li> <li>• Young's Modulus by Single Cantilever</li> <li>• Transistor Characteristics</li> <li>• Wavelength of LASER using Diffraction Grating</li> <li>• Parallel LCR Resonance Circuit</li> <li>• Black Box Experiment</li> <li>• PHET Interactive Simulation</li> <li>• Magnetic Field along the Axis of the Coil</li> </ul>
2	Engineering Chemistry Lab	<ul style="list-style-type: none"> <li>• Conductometric estimation of acid mixture</li> <li>• Potentiometric estimation of FAS using <math>K_2Cr_2O_7</math></li> <li>• Determination of pKa of vinegar using pH sensor (Glass electrode)</li> <li>• Estimation of total hardness of water by EDTA method</li> <li>• Estimation of Copper present in electroplating effluent by optical sensor (colorimetry)</li> <li>• Determination of Viscosity coefficient of lubricant (Ostwald's viscometer)</li> <li>• Determination of Chemical Oxygen Demand (COD) of industrial waste water sample</li> <li>• Estimation of Sodium present in soil/effluent sample using flame photometry</li> <li>• Synthesis of Iron-oxide Nanoparticles (Common to all branches)</li> <li>• Electrolysis of water (CSE Stream)</li> <li>• Determination of strength of an acid in Pb-acid battery ( C S E &amp; E C Stream)</li> </ul>
3	Elements of Mechanical Engg. Lab	<ul style="list-style-type: none"> <li>• Performing facing, plain turning and step turning operations by using a lathe.</li> </ul>

		<ul style="list-style-type: none"> <li>• Performing facing, plain turning and knurling operations by using a lathe.</li> <li>• Preparation of welded joints using the arc welding process.</li> <li>• Calibration of Vernier caliper and micrometer using slip gauges.</li> <li>• Determination of the angle of a specimen using a sine bar.</li> <li>• Determination of the hardness of materials using hardness testing machine.</li> <li>• Comparative study of flash point and fire point of various fuels / oils using the open cup method</li> <li>• Comparative study of flash point and fire point of various fuels / oils using the closed cup method</li> <li>• Comparative study on viscosity of different base fuels.</li> <li>• Investigation of the effect of additives on the viscosity of base fuels.</li> <li>• Selection and justification of appropriate joining techniques for given applications</li> <li>• Fabrication of a sheet metal part with simple geometry and soldering.</li> </ul>
4	Analog and Digital System Design Lab	<ul style="list-style-type: none"> <li>• Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.</li> <li>• Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator</li> <li>• Design and set up the circuits using opamp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator</li> <li>• Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches(ii) by generating digital inputs using mod-16</li> <li>• Design and implement (a) Half Adder &amp; Full Adder using basic gates and NAND gates, (b)</li> </ul>

		<p>Half subtractor &amp; Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX).</p> <ul style="list-style-type: none"> <li>• Realize (i) Binary to Gray code conversion &amp; vice-versa (IC74139), (ii) BCD to Excess-3 code conversion</li> <li>• a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.</li> <li>• Realize a) Design Mod – N Synchronous Up Counter &amp; Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC7490 / 7476 c) Synchronous counter using IC74192</li> </ul>
5	LabVIEW	<ul style="list-style-type: none"> <li>• Basic arithmetic operations: addition, subtraction, multiplication and division</li> <li>• Boolean operations: AND, OR, XOR, NOT and NAND</li> <li>• Sum of ‘n’ numbers using ‘for’ loop</li> <li>• Factorial of a given number using ‘for’ loop</li> <li>• Determine square of a given number</li> <li>• Factorial of a given number using ‘while’ loop</li> <li>• Sorting even numbers using ‘while’ loop in an array</li> <li>• Finding the array maximum and array minimum</li> </ul>
6	Verilog -XILINX	<ul style="list-style-type: none"> <li>• To simplify the given Boolean expressions and realize using Verilog program</li> <li>• To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.</li> <li>• To realize 4-bit ALU using Verilog program.</li> <li>• To realize the following Code converters using Verilog Behavioral description a)Gray to binary and vice versa b)Binary to excess3 and vice versa</li> </ul>

		<ul style="list-style-type: none"> <li>• To realize using Verilog Behavioral description: 8:1 mux, 8:3 encoder, Priority encoder</li> <li>• To realize using Verilog Behavioral description: 1:8 Demux, 3:8 decoder, 2-bit Comparator</li> <li>• To realize using Verilog Behavioral description:</li> <li>• Flip-flops: a) JK type b) SR type c) T type and d) D type</li> <li>• To realize Counters-up/down (BCD and binary) using Verilog Behavioural description.</li> </ul>
7	PSPICE	<ul style="list-style-type: none"> <li>• Design and Test (i) Bridge Rectifier with Capacitor Input Filter ii) Zener voltage regulator</li> <li>• Design and Test Biased Clippers-a) Positive, b) Negative, c) Positive-Negative d) Positive and Negative Clampers with and without Reference</li> <li>• Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor</li> <li>• Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.</li> <li>• Design and test Emitter Follower</li> <li>• Design and plot the frequency response of Common Source JFET/MOSFET amplifier</li> <li>• Test the Op amp Comparator with zero and non-zero reference and obtain the hysteresis curve</li> <li>• Design and test Full wave Controlled rectifier using RC triggering circuit</li> <li>• Design and test Precision Half wave and full wave rectifiers using Op amp</li> <li>• Design and test RC phase shift oscillator</li> </ul>

	Artificial Intelligence	<ul style="list-style-type: none"> <li>• Implement and Demonstrate Depth First Search Algorithm on Water Jug Problem</li> <li>• Implement and Demonstrate Best First Search Algorithm on Missionaries-Cannibals Problems using Python</li> <li>• Implement A* Search algorithm</li> <li>• Implement AO* Search algorithm</li> <li>• Solve 8-Queens Problem with suitable assumptions</li> <li>• Implementation of TSP using heuristic approach</li> <li>• Implementation of the problem solving strategies: either using Forward Chaining or Backward Chaining</li> <li>• Implement resolution principle on FOPL related problems</li> <li>• Implement Tic-Tac-Toe game using Python @# 16032024</li> <li>• Build a bot which provides all the information related to text in search box</li> <li>• Implement any Game and demonstrate the Game playing strategies</li> </ul>
	Digital Design and Computer Organization	<ul style="list-style-type: none"> <li>• Given a 4-variable logic expression, simplify it using appropriate technique and simulate the same using basic gates.</li> <li>• Design a 4 bit full adder and subtractor and simulate the same using basic gates.</li> <li>• Design Verilog HDL to implement simple circuits using structural, Data flow and Behavioural model.</li> <li>• Design Verilog HDL to implement Binary Adder-Subtractor – Half and Full Adder, Half and Full Subtractor.</li> <li>• Design Verilog HDL to implement Decimal adder.</li> </ul>

		<ul style="list-style-type: none"> <li>• Design Verilog program to implement Different types of multiplexer like 2:1, 4:1 and 8:1.</li> <li>• Design Verilog program to implement types of De-Multiplexer.</li> <li>• Design Verilog program for implementing various types of Flip-Flops such as SR, JK and D.</li> </ul>
	Operating Systems	<ul style="list-style-type: none"> <li>• Develop a c program to implement the Process system calls (fork (), exec(), wait(), create process, terminate process)</li> <li>• Simulate the following CPU scheduling algorithms to find turnarou nd time and waiting time a) FCFS b) SJF c) Round Robin d) Priority.</li> <li>• Develop a C program to simulate producer-consumer problem using semaphores.</li> <li>• Develop a C program which demonstrates interprocess communication between a reader process and a writer process. Use mkfifo, open, read, write and close APIs in your program.</li> <li>• Develop a C program to simulate Bankers Algorithm for DeadLock Avoidance.</li> <li>• Develop a C program to simulate the following contiguous memory allocation Techniques: a) Worst fit b) Best fit c) First fit.</li> <li>• Develop a C program to simulate page replacement algorithms: a) FIFO b) LRU</li> <li>• Simulate following File Organization Techniques a) Single level directory b) Two level directory</li> <li>• Develop a C program to simulate the Linked file allocation strategies.</li> <li>• Develop a C program to simulate SCAN disk scheduling algorithm.</li> </ul>
	Computer Networks	<ul style="list-style-type: none"> <li>• Implement three nodes point – to – point network with duplex links between them. Set</li> </ul>

		<p>the queue size, vary the bandwidth, and find the number of packets dropped.</p> <ul style="list-style-type: none"> <li>• Implement transmission of ping messages/trace route over a network topology consisting of 6 nodes and find the number of packets dropped due to congestion.</li> <li>• Implement an Ethernet LAN using n nodes and set multiple traffic nodes and plot congestion window for different source / destination.</li> <li>• Develop a program for error detecting code using CRC-CCITT (16- bits).</li> <li>• Develop a program to implement a sliding window protocol in the data link layer.</li> <li>• Develop a program to find the shortest path between vertices using the Bellman-Ford and path vector routing algorithm.</li> <li>• Using TCP/IP sockets, write a client – server program to make the client send the file name and to make the server send back the contents of the requested file if present.</li> <li>• Develop a program on a datagram socket for client/server to display the messages on client side, typed at the server side.</li> <li>• Develop a program for a simple RSA algorithm to encrypt and decrypt the data.</li> <li>• Develop a program for congestion control using a leaky bucket algorithm.</li> </ul>
	Microcontrollers & Embedded Systems	<ul style="list-style-type: none"> <li>• Develop a program to multiply two 16 bit binary numbers.</li> <li>• Write a program to find the sum of first 10 integer numbers.</li> <li>• Write a program to find factorial of a number.</li> <li>• Write a program to add an array of 16 bit numbers and store the 32 bit result in internal RAM</li> <li>• Write a program to find the square of a number (1 to 10) using look-up table.</li> </ul>

		<ul style="list-style-type: none"> <li>• Write a program to find the largest/smallest number in an array of 32 numbers .</li> <li>• Display “Hello World” message using Internal UART.</li> <li>• Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction</li> <li>• Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay in between</li> <li>• Interface a 4x4 keyboard and display the key code on an LCD.</li> </ul>
	Scala	<ul style="list-style-type: none"> <li>• Write a Scala program to compute the sum of the two given integer values. If the two values are the same, then return triples their sum.</li> <li>• Write a Scala program to check two given integers, and return true if one of them is 22 or if their sum is 32.</li> <li>• Write a Scala program to remove the character in a given position of a given string. The given position will be in the range 0...string length -1 inclusive.</li> <li>• Write a Scala program to create a new string taking the first 5 characters of a given string and return the string with the 5 characters added at both the front and back.</li> <li>• Write a Scala program to print the multiplication table of a given number using a for loop.</li> <li>• Write a Scala program to find the largest element in an array using pattern matching</li> <li>• Write a Scala function to calculate the product of digits in a given number</li> <li>• Write a Scala function to check if a given number is a perfect square</li> <li>• Write a Scala program that creates a subclass Student that extends the Person class. Add a property called grade and implement methods to get and set it.</li> </ul>

		<ul style="list-style-type: none"> <li>• Write a Scala program that creates a class Triangle with properties side1, side2, and side3. Implement a method is Equilateral to check if the triangle is equilateral.</li> <li>• Write a Scala program that creates an enum class Color with values for different colors. Use the enum class to represent an object's color.</li> <li>• Write a Scala program that creates a class ContactInfo with properties name, email, and address. Create a class Customer that includes a ContactInfo object.</li> <li>• Write a Scala program to create a set and find the difference and intersection between two sets.</li> <li>• Write a Scala program to create a set and find the second largest element in the set.</li> <li>• Write a Scala program to create a list in different ways. Note: Use Lisp style, Java style, Range list, Uniform list, Tabulate list</li> <li>• Write a Scala program to flatten a given List of Lists, nested list structure.</li> <li>• Write a Scala program to add each element n times to a given list of integers.</li> <li>• Write a Scala program to split a given list into two lists.</li> <li>• Write a Scala program to swap the elements of a tuple Further print no swapping required if elements are same.</li> <li>• Write a Scala program to find non-unique elements in a tuple</li> </ul>
	Digital Communication Lab	<ul style="list-style-type: none"> <li>• Generation and demodulation of the Amplitude Shift Keying signal.</li> <li>• Generation and demodulation of the Phase Shift Keying signal.</li> <li>• Generation and demodulation of the Frequency Shift Keying signal.</li> <li>• Generation of DPSK signal and detection of data using DPSK transmitter and receiver.</li> </ul>

		<ul style="list-style-type: none"> <li>• Simulation Experiments</li> <li>• Gram-Schmidt Orthogonalization: To find orthogonal basis vectors for the given set of vectors and plot the orthonormal vectors.</li> <li>• Simulation of binary baseband signals using a rectangular pulse and estimate the BER for AWGN channel using matched filter receiver.</li> <li>• Perform the QPSK Modulation and demodulation. Display the signal and its constellation.</li> <li>• Generate 16-QAM Modulation and obtain the QAM constellation.</li> <li>• Encoding and Decoding of Huffman code.</li> <li>• Encoding and Decoding of binary data using a Hamming code.</li> <li>• For a given data, use CRC-CCITT polynomial to obtain the CRC code. Verify for the cases, a) Without error b) With error</li> <li>• Encoding and Decoding of Convolution code</li> </ul>
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**13.13 Innovation Cell:** Yes

**13.14 Social Media Cell:** Yes

**13.15 To upload the respective short video (1-2 min) of Infrastructure and facilities available w.r.t the courses in the website:** Yes

**13.16 Games and Sports Facilities**

- **Indoor Sports facilities:** Table Tennis, Chess, Carom
- **Outdoor Sports facilities:** Football (Lawn Ground), Volleyball (1 courts), Basketball (two courts), Tennis (two courts), Kabaddi, Swimming pool, Pavilion

**13.17 Extra-Curricular Activities:** Cultural Cell available

**13.18 Teaching Learning Process**

- Curriculum and syllabus for each of the Programmes as approved by the University [www.vtu.ac.in](http://www.vtu.ac.in)
- Academic Calendar of the University – as per VTU.
- Academic Time Table: Available

- Teaching Load of each Faculty: As per Standard Norms
- Internal Continuous Evaluation System: Yes
- Student's Assessment of Faculty, System in place: Yes

**13.19 For each Post Graduate Courses give the following**

Title of the Course: MBA and MCA

Laboratory facilities exclusive to the Post Graduate Course: 01

**13.20 MoUs with Industries: Yes**

  
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